Available online at www.sciencedirect.com

ScienceDirect

Journal of Electrical Systems and Information Technology 3 (2016) 398–410

www.elsevier.com/locate/jesit

An extended dual input dual output three level *Z* source inverter with improved switch loss reduction technique

N.B. Deshmukh *, R.D. Thombare, M.M. Waware, D.S. More

Department of Electrical Engineering, Walchand College of Engineering, Sangli, India

Received 14 March 2016; received in revised form 5 July 2016; accepted 20 July 2016
Available online 11 August 2016

Abstract

Multilevel inverter (MLI) is a proven technology used for industrial applications due to low output total harmonic distortion (THD), high power handling capability and low active device rating. Dual output inverter is a recent trend associated with inverter topologies for specialized applications. This paper deals with three phase three level dual input dual output inverter topology with minimum active device count. Reduction in switch count leads to reduction in losses and improves reliability. Both the input sources share power equally as neutral point current ripple is maintained low. For further reduction in switching losses at higher switching frequencies, the concept of "no switching zone" or discontinuous pulse width modulation (DPWM) has been put forth recently. This paper proposes modification in the placement of "no switching zone" in order to optimize switching losses and output THD (output filtering requirements) for low power factor load. This study also proposes novel graphical approach to analyze the loss reduction along with its effect on output THD. The sinusoidal PWM (SPWM) is used which gives satisfactory switching loss reduction without complex calculations. Moreover, the proposed topology is generalized to provide dual output at higher voltage levels. It is seen that the components reduction phenomenon becomes more pronounced as number of levels goes on increasing. The proposed converter is simulated in MATLAB software environment and results are obtained.

Keywords: Dual input dual output three level inverter; Loss area; "No switching zone"; SPWM; *Z* source network

1. Introduction

Presently multilevel inverters are the preferred choice for high-voltage and high-power applications in industry. There are different topologies have been reported for multilevel inverters depending upon level of output voltage, number of inputs/outputs and number of active semiconductor devices. These are cascaded multilevel inverter, generalized

* Corresponding author.
E-mail addresses: nbd.nmt@gmail.com (N.B. Deshmukh), vrthombare@gmail.com (R.D. Thombare).
Peer review under responsibility of Electronics Research Institute (ERI).

Production and hosting by Elsevier

http://dx.doi.org/10.1016/j.jesit.2016.07.003

Nomenclature

List of symbols

L-L line t line
SW1 to SW9 IGBT switches
SW10 to SW27 bidirectional IGBT switches
M1 Method 1
M2 Method 2
M3 Method 3
Vs1 Voltage Source 1
Vs2 Voltage Source 2
Vs3 Voltage Source 3
Vs4 Voltage Source 4
C1 and C2 capacitors
L1 and L2 inductors
VR, VY and VB three phase voltages

multilevel converter/inverter topology and its derivations to other topologies (diode clamped, flying capacitors, modular multilevel converter and Marx multilevel converter, etc.) (Peng et al., 2010; Mittal et al., 2012).

Single input dual output nine-switch inverter that can independently control amplitude and frequency for two three phase loads is proposed (Kominami and Fujimoto, 2007). A dual input dual output *Z*-source inverter is proposed (Dehghan et al., 2010). This inverter can control two AC load using two DC sources. A nine-switch three-level *Z*-source inverter is proposed which reduces the number of switches and retains capabilities such as voltage boosting and low harmonic content (Masoudian and Farjah, 2013). A new inverter having two three-phase three-level outputs is presented (Haruna and Hoshi, 2014). The proposed inverter can drive two permanent magnet synchronous motor (PMSMs) with three-level phase voltage having less voltage and current harmonics distortion and the voltage stress of each switching devices. A single DC source inverter handling phase and magnitude of the two AC outputs with different frequencies is proposed (Scott et al., 2014). However, the above mentioned topologies fail to provide dual outputs and line to line three level voltages with minimum switch count as shown in Table 1.

Switching losses is a dominating factor in total losses as switching frequency goes on increasing. There are two methods available for reducing the switching losses. First method is by employing new type of switching technique such as zero current switching (ZCS) or zero voltage switching (ZVS) that require additional hardware.

Another method to reduce the switching losses by using advanced PWM control techniques like selective harmonic elimination, and space-vector pulse width modulation (SVPWM) that require the complex mathematical calculations. A new PWM method for the three-level inverter with an ability to reduce the switching loss is introduced (Kaku et al., 1997). The reduced switching loss closed loop PWM technique is proposed to reduce switching losses without

Table 1
Comparison of different MLI topologies.

Multilevel inverter topologies	No. of O/Ps	O/P voltage level (L-L)	No. of active devices
Diode clamped MLI (Peng et al., 2010; Mittal et al., 2012)	1	3	12
Flaying Capacitor MLI (Peng et al., 2010; Mittal et al., 2012)	1	3	12
Cascaded MLI (Peng et al., 2010; Mittal et al., 2012)	1	3	24
Generalized MLI (Peng et al., 2010; Mittal et al., 2012)	1	3	18
Nine switch Inverter (Kominami and Fujimoto, 2007)	2	2	9
Modified nine switch inverter (Dehghan et al., 2010)	2	2	9
Nine switch three level inverter (Masoudian and Farjah, 2013)	1	3	9
Three-level twin drive inverter (Haruna and Hoshi, 2014)	2	3	21
Three level Marx Inverter (Scott et al., 2014)	2	3 and 2	15
Proposed three level inverter	2	3	15

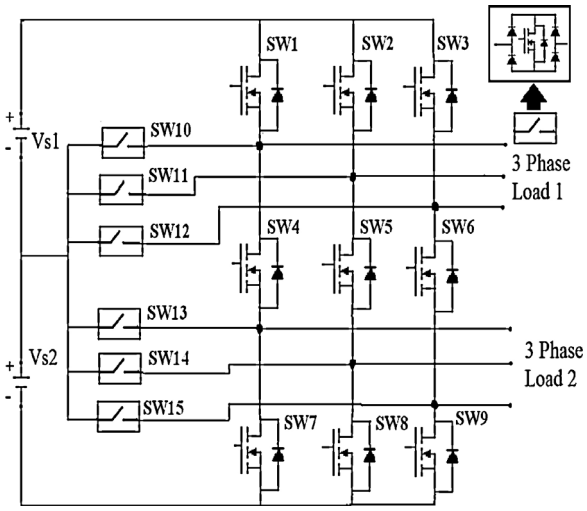

Fig. 1. Proposed dual input three level dual output inverter.

sensing load power factor angle (Chaturvedi et al., 2011). The carrier-based neutral point potential (NPP) regulator is designed so as to effectively reduce the switching losses of the three-level inverter without any complex mathematical expressions (Chaturvedi et al., 2014). A novel randomized control strategy for three-phase voltage source inverters is described (Trrynadlowski et al., 1997). In this control strategy, an implicit asymmetrical modulating function results in switching losses in the inverter being reduced by about half in comparison with those using the classical space vector pulse width modulation method.

In this paper, an extended dual input dual output three level inverter topology is proposed. To obtain three level output voltage a topological modification is done in conventional nine switch inverter by connecting six bidirectional switches in between sources and nine switches as shown in Fig. 1. *Z* source is integrated with sources and proposed inverter to provide buck-boost operation from DC link as shown in Fig. 2. The reduction of power switches will reduce system cost and improve the efficiency as well as reliability. The comparison of different MLI topologies with respect to no. of outputs, line to line output voltage level and no. of active devices required is given in Table 1.

To improve the system efficiency, reduction of switching losses is most desirable; as at higher switching frequency switching losses become dominant. The sinusoidal pulse width modulation technique is used to control the proposed

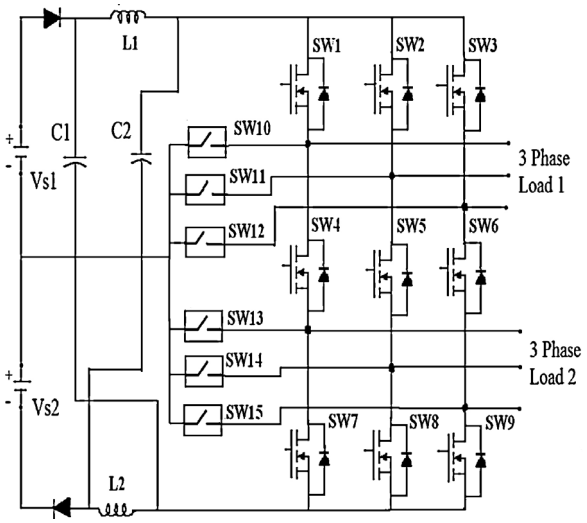

Fig. 2. Proposed dual input three level dual output inverter with *Z* source network.

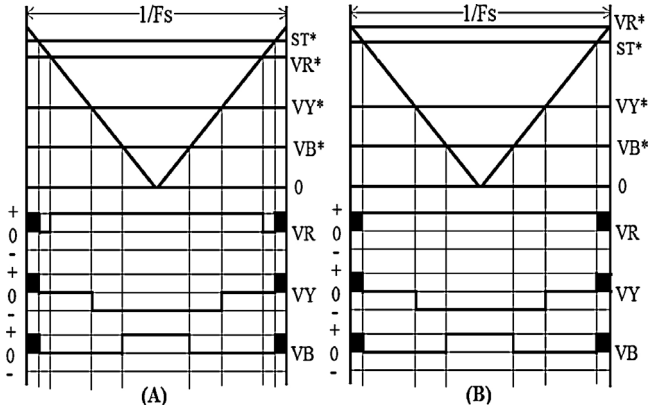

Fig. 3. Switching signal generation using modified sine waves and triangular waves.

converter. The concept of "no switching zone" is proposed recently. The researchers have placed this "no switching zone"/"dead band" of 60° at the peak of fundamental load voltage and fundamental load current (Kaku et al., 1997; Chaturvedi et al., 2011, 2014; Trrynadlowski et al., 1997). The drawbacks associated with these methods are as follows: In case of placing "no switching zone" at peak of load voltage, output THD is minimum yet the switching loss reduction is not significant for low power factor load. In case of placing "no switching zone" at peak of load current, the switching loss reduction is significant at all load power factors yet the output THD is poor. The study presents an optimized solution of placing "no switching zone" at the peak of fundamental load power and gives graphical analysis to support the conclusions.

Impedance source networks (ZS) and their applications are not authors' contributory work and hence are out of scope of this study. For further clarification, readers are requested to go through (Siwakoti et al., 2015a,b).

2. Control technique for proposed inverter

The control technique of the proposed topology is a combination of the control techniques proposed for nine switch dual output inverter and nine switch three level inverter. Here there are two modified sine waves and two triangular waves (per phase) used for comparison. Upper sine wave is always compared with upper triangular wave. Lower sine wave is always compared with lower sine wave. There are two sinusoidal envelopes with frequency thrice that of modulating sinusoidal signal are used to generate the shoot through state. When the upper triangular wave is greater than the upper envelope or when the lower triangular wave is lesser than the lower envelope, shoot through (ST) state is applied (Siwakoti et al., 2015a,b). Here when upper sine wave is greater than the upper triangular wave, SW1 is turned on. When lower sine wave is lesser than the lower triangular wave, SW7 is turned on. The pulses given to SW4 are logic XOR of the pulses given to SW1 and SW7. The pulses given to SW10, SW13 are same and they are obtained by logic NOR of the pulses given to SW1 and SW7. In case of shoot through state, SW1 to SW9 are closed and SW10 to SW15 are opened. Fig. 3(A) shows switching of inverter phases based on sine carrier comparison. Fig. 3(B) shows switching of inverter phases based on sine carrier comparison in "no switching zone". "+" sign indicates phase being connected to positive maxima of input voltage whereas "−" sign indicates phase being connected to negative maxima of input voltage. "0" sign indicates phase being connected to the neutral point or midpoint of input voltage sources.

3. Switching loss calculation

Consider the switching waveforms of the insulated gate bipolar transistor (IGBT) voltage V_{CE} and the current I_E, corresponding to the turn- on and turn-off time. During each transition from on to off, and vice versa, the transistor has simultaneously high voltage and current, as per the switching waveforms. The instantaneous power loss $P_{SW}(t)$ in

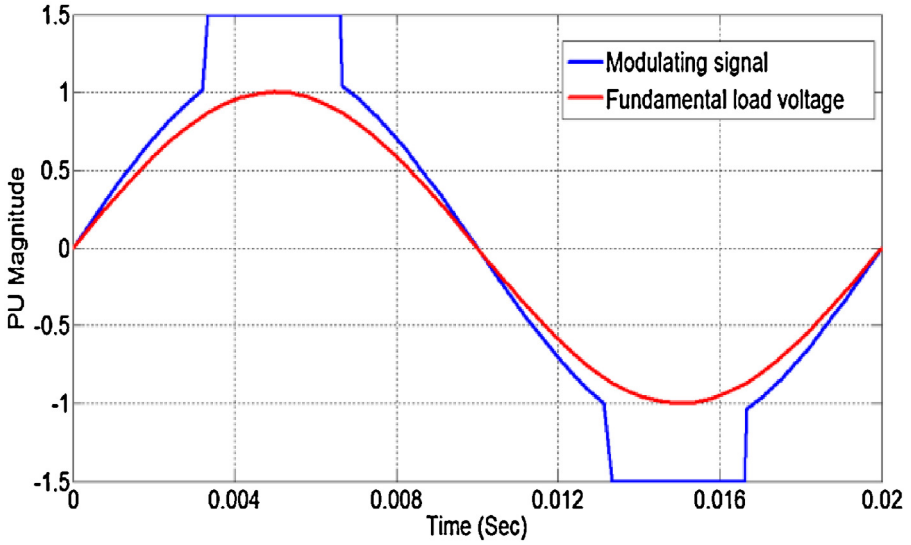

Fig. 4. No switching zone for fundamental load voltage.

the transistor is the product of V_{CE} and $I_{E.}$ Then the switching power loss for one fundamental waveform is given as Eq. (1)

$$P_{SW}(t) = \frac{1}{2} V_{in} I_o (t_C(\text{on}) + t_C(\text{off}))\, fs \tag{1}$$

where t_C(on) and t_C(off) are the rise and the fall times associated with the IGBT voltage and current, V_{in} is the DC link voltage seen by switch during transition, I_o is the load current flowing through switch and *fs* is the switching frequency (Mohan, 2003).

4. Analysis of switching losses

Switching frequency selection is a trade-off between switching losses and output harmonic performance. Under these circumstances, it is highly desirable to reduce switching losses by using appropriate placement of "no switching zone".

To reduce the switching losses, there is insertion of "no switching" zone within each half cycle of fundamental wave. In the "no switching zone" of a particular switch, the switch is made continuously turned on. Using the proposed method, every phase of the inverter can be continuously switched on for 120° of which 60° for positive half cycle and 60° for negative half cycle.

This "no switching zone" can be placed in accordance with

Method 1: Peak of fundamental load voltage.
Method 2: Peak of fundamental load current.
Method 3: Peak of fundamental load power.

Here a "no switching zone" of 60° is introduced to each switch SW1 to SW3 and SW7 to SW9. So there are six "no switching zones", each of the duration 60° symmetrically placed in a complete cycle of 360°. Due to such placement, switching of SW1 to SW3 and SW7 to SW9 is reduced by 16.66% of a cycle; Switching of SW4 to SW6 and SW10 to SW15 are reduced by 33.33% of a cycle. The positions of "no switching zone" are given by Figs. 4–6.

The voltage across the switch during transition will always remain the same; it is assumed to be 1 p.u. (per unit). The load current supplied by switch will vary in sinusoidal fashion. The product of these quantities will be directly

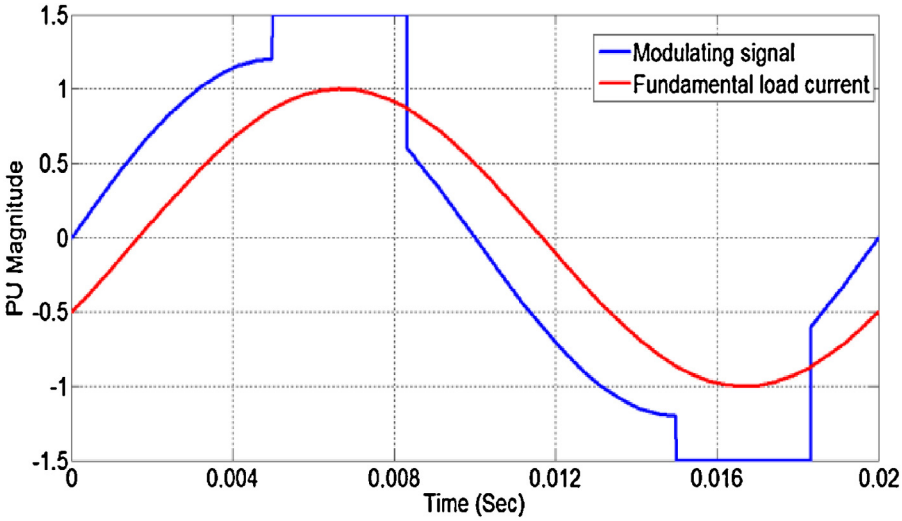

Fig. 5. No switching zone for fundamental load current.

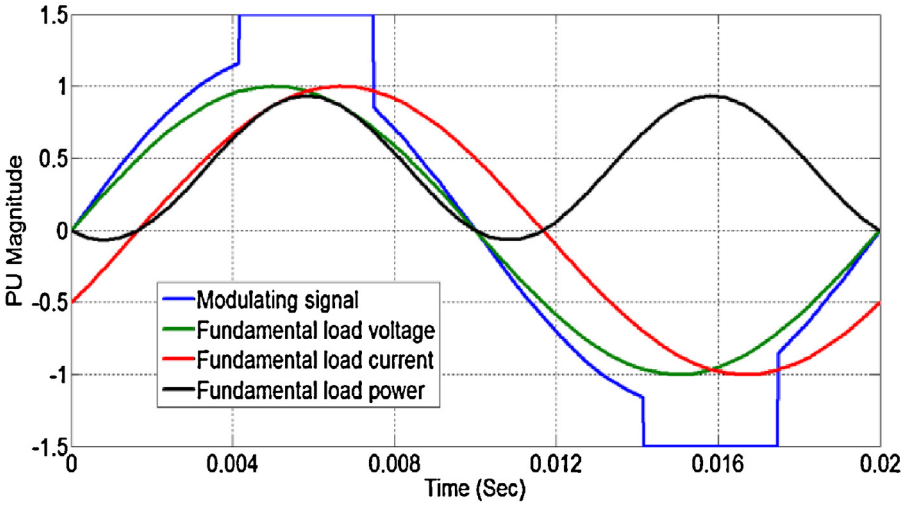

Fig. 6. No switching zone for fundamental load power.

proportional to the switching power loss taking place in switch in one fundamental cycle, as seen from Eq. (1). If product of power and time is considered; it can be concluded that the nature of instantaneous energy loss in the switches is equivalent to the net magnitude of area enclosed by the power curve with time axis. This basis is used for comparison of losses.

When a "no switching zone" is inserted, the switching power loss will be replaced by conduction losses as the switch is made continuously on. Conduction losses are very less, when compared to switching losses at very high switching frequencies and low load current applications. Therefore, total losses in the "no switching zone" are assumed to be approximately zero.

From the total area enclosed by power curve with *X* axis is subtracted by the area that comes under "no switching zone", an area is obtained proportional to the switching energy losses in one fundamental cycle. It is termed as loss area of that particular method. Loss areas are compared for Method 1, Method 2 and Method 3 which is shown in Figs. 7–9 respectively. The method having least loss area will be the most effective in terms of switching loss reduction. As "no switching zone" is placed symmetrically in positive and negative half of the fundamental wave, calculations

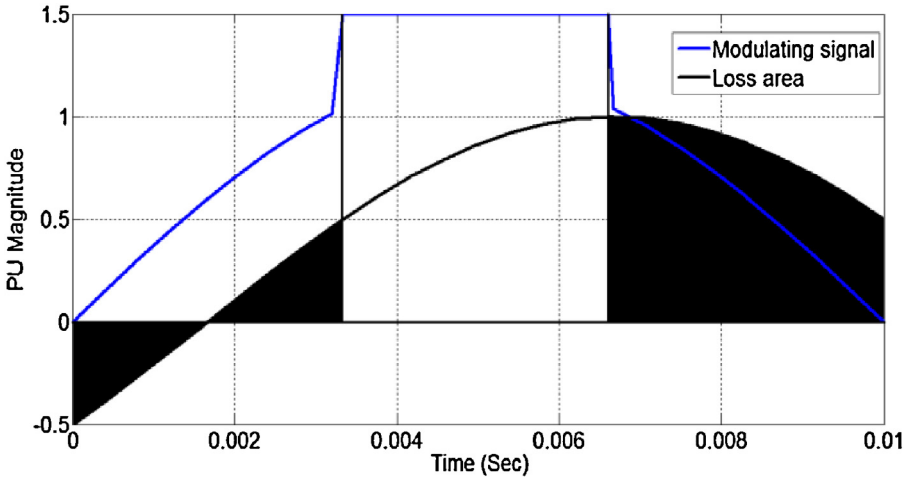

Fig. 7. Loss area with Method 1.

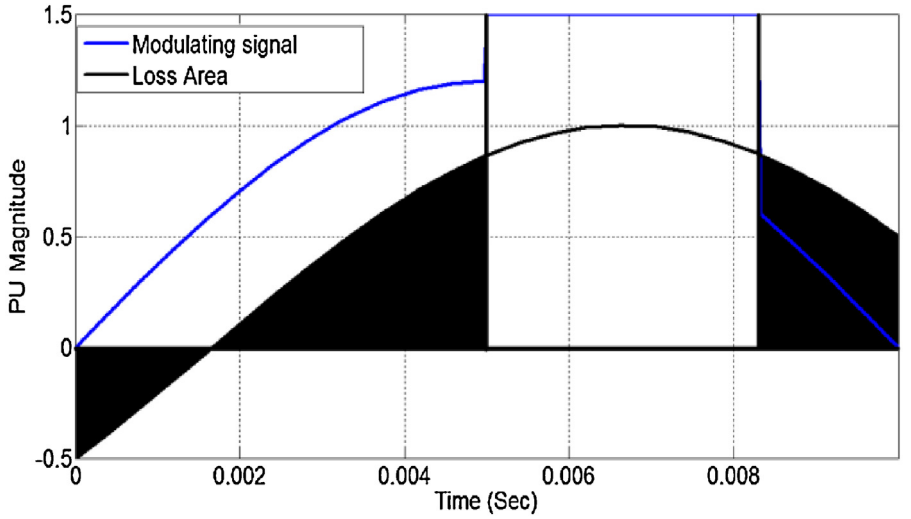

Fig. 8. Loss area with Method 2.

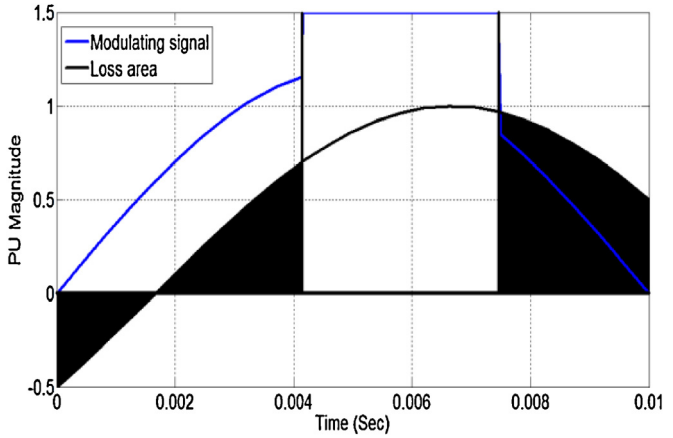

Fig. 9. Loss area with Method 3.

are restricted to positive half cycle only. Taking help of the symmetry of the waveform, it is possible to extend the calculations.

Let θ be the angle by which fundamental load voltage leads fundamental load current.

For $\theta < 60^\circ$,

Loss area of conventional SPWM method, termed as A_1

$$y(x) = 1\ \sin(x - \theta) \tag{2}$$

$$A_1 = 2\left[\int_{\theta}^{\pi} y dx - \int_{0}^{\theta} y dx\right] \tag{3}$$

Loss area of Method 1 is

$$= 2\left[\frac{A_1}{2} - \int_{\pi/3}^{2\pi/3} y dx\right] \tag{4}$$

Loss area of Method 2 is

$$= 2\left[\frac{A_1}{2} - \int_{((\pi/3)+\theta)-(\pi/6)}^{((\pi/2)+\theta)+(\pi/6)} y dx\right] \tag{5}$$

Loss area of Method 3 is

$$= 2\left[\frac{A_1}{2} - \int_{((\pi+\theta)/2)-(\pi/6)}^{((\pi+\theta)/2)+(\pi/6)} y dx\right] \tag{6}$$

For $\theta > 60^\circ$, let the loss area of conventional SPWM method is termed as A_2

$$A_2 = 2\left[\int_{\theta}^{\pi} y dx - \int_{0}^{\theta} y dx\right] \tag{7}$$

Loss area of Method 1 is

$$= 2\left[\frac{A_2}{2} - \left[\int_{\theta}^{2\pi/3} y dx - \int_{\pi/3}^{\theta} y dx\right]\right] \tag{8}$$

Loss area of Method 2 is

$$= 2\left[\frac{A_2}{2} - \left[\int_{((\pi+\theta)/2-(\pi/6)}^{\pi} y dx - \int_{\pi}^{((\pi+\theta)/2+(\pi/6)} y dx\right]\right] \tag{9}$$

Loss area of Method 3 is

$$= 2\left[\frac{A_2}{2} - \int_{((\pi/2)+(\theta/2))-(\pi/6)}^{((\pi/2)+(\theta/2))+(\pi/6)} y d\theta\right] \tag{10}$$

Now effectiveness of three methods are compared as per load power factor variation at fixed switching frequency with voltage and current kept constant at 1 p.u. Fig. 10 shows the percentage loss area of each method when loss area of Method 2 is considered as 100%. The Variation is shown for 60° lagging power factor angle to 60° leading power factor angle.

5. Effects of loss reduction methods on output THD

The modulating signal is true replica of the output fundamental voltage. Hence, it is considered that the output voltage THD is directly proportional to the THD of modulating signal. Here carrier frequency components of output voltage are ignored as carrier frequency is kept constant for all loss reduction methods. Fig. 11 shows the percentage output THDs (Y axis) of each method when load and other circuit parameters are kept same. The variation is shown for 60° lagging power factor angle to 60° leading power factor angle.

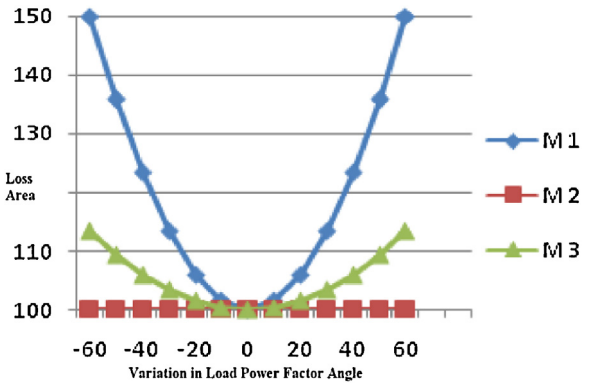

Fig. 10. Comparison of Method 1 (M1), Method 2 (M2), Method 3 (M3).

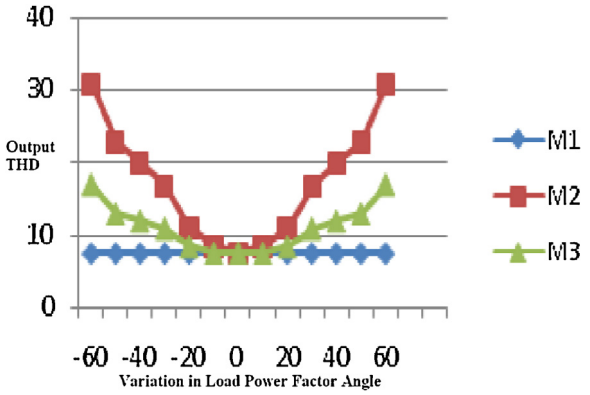

Fig. 11. Comparison of Method 1 (M1), Method 2 (M2) and Method 3 (M3).

6. Extension of proposed converter structure

The proposed dual output converter can be seen as insertion of bidirectional switches to basic nine switch topology to increase the voltage levels in output. These switches are connected to the midpoint of the DC link to ensure the equal magnitude of voltage steps in output voltage waveform. This concept can be extended by further division of DC link and connection of bidirectional switches from each point to each output. Five level (nine levels in line to line voltage) dual output concept is shown in the Fig. 12. The DC link is now divided in four equal parts and bidirectional switches are inserted to increase the output voltage levels. Similarly the proposed concept can theoretically be extended to form *N* number dual output structure.

The reduction in the number of components becomes more significant as level goes on increasing. If five level dual output is to be generated by diode clamped concept, 48 switches and large number of clamping diodes will be required. If five level dual output is to be generated by flying capacitor concept, 48 switches and large number of flying capacitors. The proposed structure uses only 27 active switches to realize the same output voltage.

The control of the five level structure is extension of SPWM technique discussed in Section 2. Three level structure requires two modified sinusoids and two carrier signals to control active switches one phase. Five level structure requires two modified sinusoids and four carrier signals to control active switches of one phase. These four carrier signals are in phase, having equal magnitude and will be spaced so as to form a continuous band. This control technique can also be easily extended to further levels facilitating easy and low cost implementation. As the number of voltage levels goes on increasing, the distribution of the P-type switching states (charging effect on capacitors) and N-type switching states (discharging effect on capacitors) is not maintained uniform. So additional computational efforts or additional circuitry might be required to balance the DC link capacitor voltages, which again is not new for multilevel inverter structures.

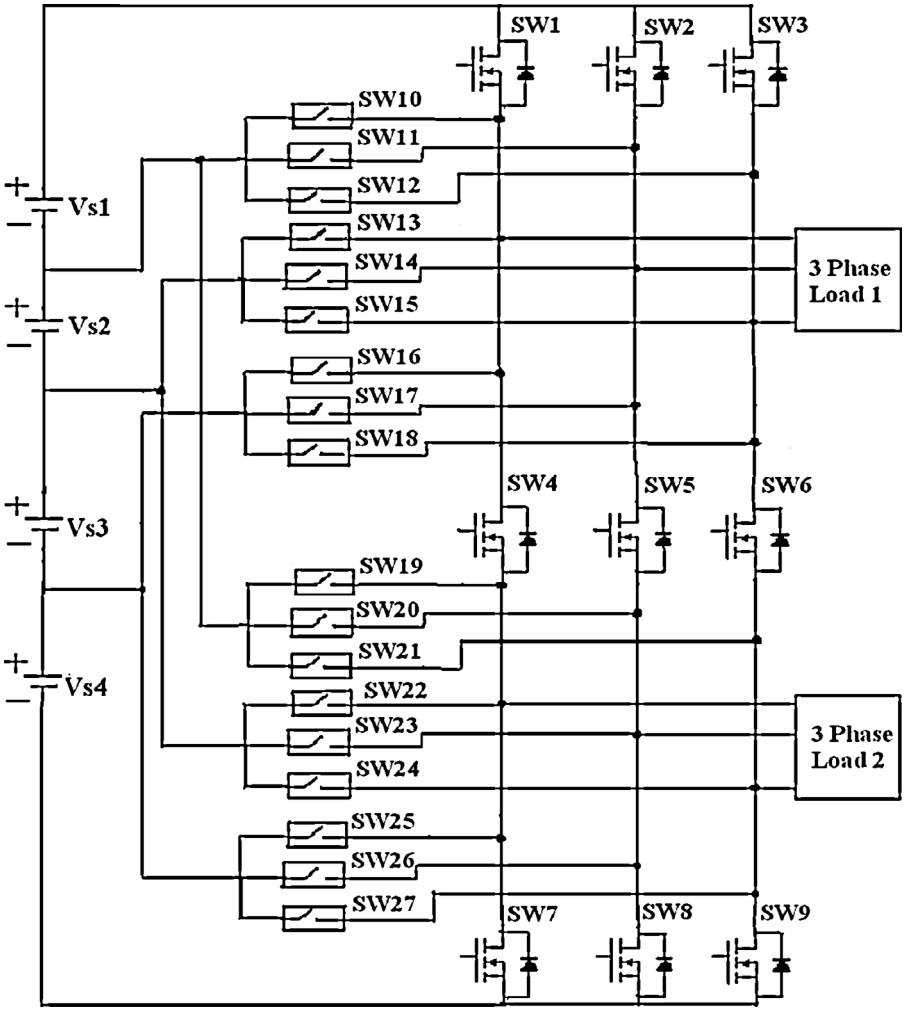

Fig. 12. An extended dual input five level dual output inverter.

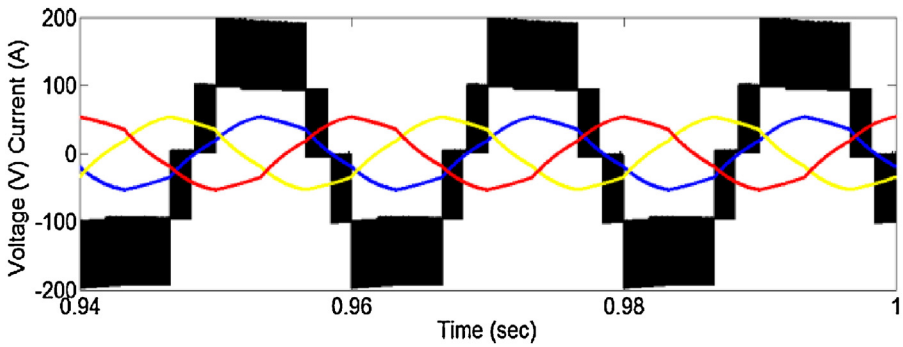

Fig. 13. Line voltage and current without *Z* source for output 1.

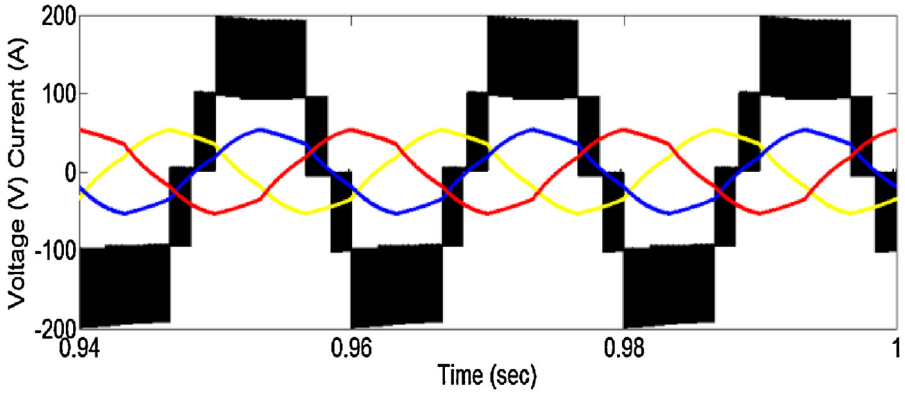

Fig. 14. Line voltage and current without *Z* source for output 2.

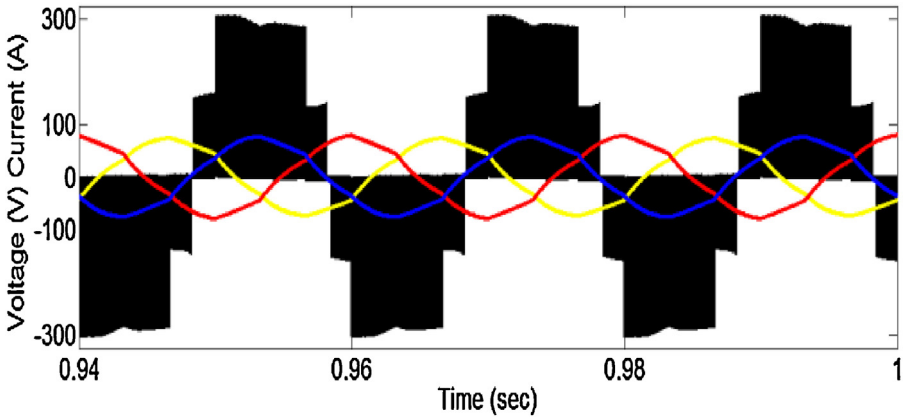

Fig. 15. Line voltage and current with M3 (output 1, ZS).

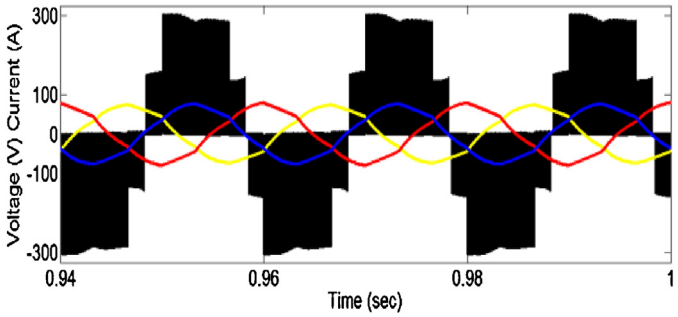

Fig. 16. Line voltage and current with M3 (output 2, ZS).

7. Simulation parameters and results

Simulation parameters used in this paper are as follows:

Input voltage Vs1 and Vs2 is 100 V each and load power factor (RL load) is 0.866. Inductors and capacitors of *Z* source network are 3 mH and 1 mF respectively. Switching frequency (*fs*) is 10 kHz and output frequency of inverter is 50 Hz. The modulation index for both outputs is 0.93.

The simulation results of proposed dual input dual output three level inverter for proposed method is shown as follows. Figs. 13 and 14 show three level line to line output voltages of output 1 and output 2 without *Z* source network and its three phase current respectively. Figs. 15 and 16 show three level line to line output voltages of output 1 and

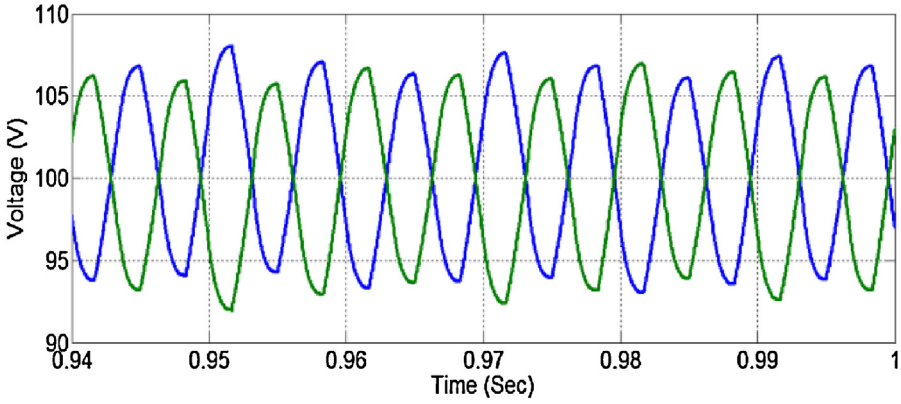

Fig. 17. input side DC link capacitor voltages.

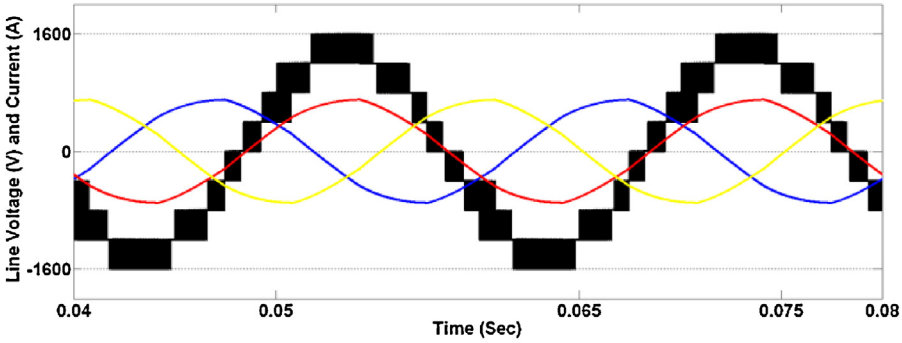

Fig. 18. Five level line to line voltage and current of output 1.

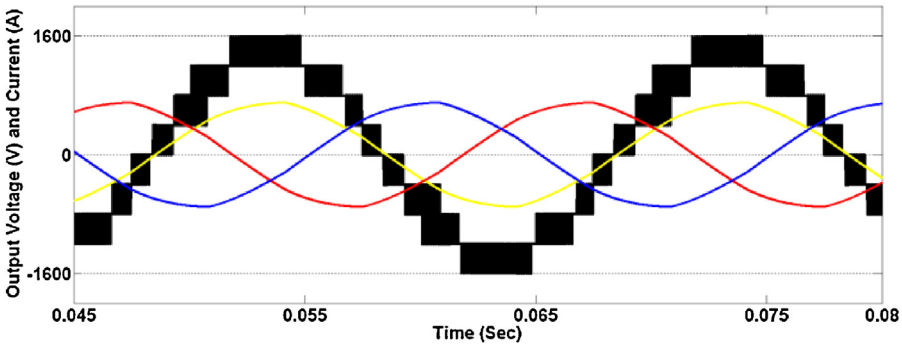

Fig. 19. Five level line to line voltage and current of output 2.

output 2 with *Z* source network and its three phase current respectively. Fig. 17 shows input side DC link capacitor voltages. The neutral point ripple is maintained low as the P-type switching states and N-type switching are distributed uniformly in each fundamental cycle. Figs. 18 and 19 show five level line to line voltages of output 1 and output 2 without *Z* source and its three phase current respectively having each voltage source (Vs1, Vs2, Vs3 and Vs4) is of 400 V.

8. Conclusion

The paper developed an extended dual input dual output three level inverter with minimum switch count. The switching loss is reduced by placing of "no switching zone" at appropriate location. The paper analyzes switching loss

reduction by conventional placement of "no switching zone" and proposes a new method with optimized switching loss reduction and output harmonic performance. From Fig. 10, it is quite clear that the loss reduction performance of proposed method is close to that of Method 2 whereas Method 2 gives least switching loss performance. From Fig. 11, it is quite clear that the output harmonic performance of proposed method is in between Method 1and Method 2 whereas Method 1 gives minimum output THD. Moreover, the proposed topology is generalized to provide dual output at higher voltage levels. It is seen that the components reduction phenomenon becomes more pronounced as number of levels goes on increasing. Despite of several advantages offered, the proposed topology suffers disadvantages such as low DC link utilization and higher device rating, which is not new for component minimized topologies. The proposed converter finds applications in renewable energy grid integration, industrial drives and home appliances with unique advantages such as high power handling capability, increased voltage level and reduced switching losses as well as switch count.

References

Chaturvedi, P.K., Jain, S., Agarwal, P., 2011. Reduced switching loss pulse width modulation technique for three-level diode clamped inverter. IET Power Electron. 4 (4), 393–399.

Chaturvedi, P., Jain, S., Agarwal, P., 2014. Carrier-based neutral point potential regulator with reduced switching losses for three-level diodeclamped inverter. IEEE Trans. Ind. Electron. 61 (2), 613–624.

Dehghan, S.M., Mohamadian, M., Yazdian, A., Ashrafzadeh, F., 2010. A dual-input–dual-output *Z*-source inverter. IEEE Trans. Power Electron. 25 (2), 360–368.

Haruna, J., Hoshi, N., 2014. A novel three level inverter which can drive two PMSMs. In: IET Intl. Conf. Power Electronics, Machines and Drives, pp. 1–6.

Kaku, B., Miyashita, I., Sone, S., 1997. Switching loss minimized space vector PWM method for IGBT three-level inverter. IEE Proc. Electr. Power Appl. 144 (3), 182–190.

Kominami, T., Fujimoto, Y., 2007. A novel nine-switch inverter for independent control of two three-phase loads. In: Industry Application Conference, pp. 2346–2350.

Masoudian, A., Farjah, E., 2013. Nine-switch three-level *Z* source inverter. In: Power Electronics, Drive Systems & Technologies Conference (PEDSTC), pp. 224–229.

Mittal, N., Singh, B., Singh, S.P., Dixit, R., Komar, D., 2012. Multi-level inverter: a literature survey on topologies and control strategies. In: ICPCES, 2nd International Conference on Power, Control and Embedded Systems, pp. 1–11.

Mohan, N., 2003. Power Electronics and Drives, ISBN: 0-9715292-2-1.

Peng, F.Z., Qian, W., Cao, D., 2010. Recent advances in multilevel converter/inverter topologies and applications. In: Conf. Rec. IEEJ Int. Power Electron. Conf., Sapporo, Japan, pp. 492–501.

Scott, M.J., Zamora, R.D., Andong, L., Cong, L., Fanbo, Z., Wang, J., 2014. Multilevel, multiport, switched-capacitor based inverter for utility applications. In: IEEE Energy Conversion Congress and Exposition (ECCE), pp. 3930–3933.

Siwakoti, Y.P., Peng, F.Z., Blaabjerg, F., Loh, P.C., Town, G.E., 2015a. Impedance-source networks for electric power conversion. Part I. A topological review. IEEE Trans. Power Electron. 30 (2), 699–716.

Siwakoti, Y.P., Peng, F.Z., Blaabjerg, F., Loh, P.C., Town, G.E., Yang, S., 2015b. Impedance-source networks for electric power conversion. Part II. Review of control and modulation techniques. IEEE Trans. Ind. Appl. 30 (4), 1887–1906.

Trrynadlowski, A.M., Kirlin, R.L., Legowski, S., 1997. Space vector PWM technique with minimum switching losses and a variable pulse rate, space vector PWM technique with minimum switching losses and a variable pulse rate. IEEE Trans. Ind. Electron. 44, 173–181.